of the mid-term result register.

Figure 19 conceptually shows changes in the contents (structure, flow) of the pipeline processing due to the provision of the second syndrome calculator 52, or how the process is speeded up. This drawing indicates that the process is speeded up by one step.

(Embodiment 8)

The present embodiment is an improvement of Embodiment 7.

In Embodiment 7 the second syndrome calculator 52 and the second error detector 72 process demodulated data only. In this case, while the second syndrome calculator 52 is performing syndrome calculation for demodulated data (a code word) one time, the second syndrome calculator 51 executes syndrome calculation for data in the buffer memory 4 twice. Thus, if these syndrome calculators have an equal capacity, the second syndrome calculator 52 will stand idle for some time.

CPU-related data require highly precise error correction, and data stored in media that have been under poor storage conditions for a long time period may demand repeated error correction. It is highly likely in such a case that if the first syndrome calculator 51 exclusively processes data in the buffer memory 4, the second syndrome calculator 52 sits idle. Hence, in the present embodiment, after the demodulated data are stored in the buffer memory 4, the second syndrome calculator 52 is also designed to perform error correction.

Figure 20 shows the structure of the main part of the error correction device of the present embodiment.

The error correction device of the present embodiment basically has

the same structure as the device of Embodiment 7 shown in Figure 18 except that the first and second syndrome calculators 51, 52 and the first and second error detectors 71, 72 are connected also to the buffer memory 4 and that selectors 301, 302 select between data immediately after demodulation and data in the buffer memory 4 as a target of process.

The control unit 300 controls the ECC block, the sector, the sector group in process, the number of strings, and the number of times of correction for each component unit (means) of the device by forming reference lists. Based on the reference lists, the control unit 300 further controls the storage of the mid-term results of error correction to an appropriate address in the mid-term result register 80, and switching operations. Figures 21A and 21B conceptually show the contents of the reference table 303. Figure 21A is a reference list containing ECC blocks and selectors which are being processed in each component unit. Figure 21B is a reference list containing the position of data which are being processed in each ECC block and the number of times of error correction.

The control unit 300 refers to these lists synchronously with clock signals, and updates the contents of these lists to make each component unit perform a necessary process. With the present invention, it is not so difficult to compose, refer, and update these lists in terms of hardware or software, so that the description of the specific contents will be omitted.

As described hereinbefore, according to the present embodiment, data before the syndrome calculators 51, 52 detect an error-containing code can be subjected to an error detecting process in parallel with syndrome calculation, which eliminates the need for all data to be transferred from

the buffer memory 4 to the first and second error correctors 71, 72 after error correction. This can reduce the time required for a sequence of error correcting process.

Pipeline processing for a plurality of ECC blocks can reduce the time required for a sequence of error correcting process.

Performing syndrome calculation and error detection with the writing of demodulated data to the buffer memory 4 can reduce the time required for a sequence of error correcting process.

Some types of data allow the writing of subsequent data to the buffer memory 4 and the transfer of error-corrected data downstream to be performed at the same time, which reduces the time required for a sequence of error correcting process.

The error correction is done in accordance with the contents and conditions of data, which reduces the time required for a sequence of error correcting process.

A combination of these processes can further reduce the time required for a sequence of error correcting process.

The present invention, which has been described based on the embodiments, is not restricted to them, and can be structured as follows.

1) Error-containing data on the buffer memory are temporarily read into the error corrector, and the error-corrected data are written back into the buffer memory. Instead of this, the address of the data on the buffer memory can be exclusively transmitted from the error corrector to the bus control unit, and the error in the data read based on the address from the buffer memory can be corrected in the bus control unit and written back to